IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (canceled)

2. (original) A semiconductor chip assembly comprising:

(a) a subassembly including a semiconductor chip having a front surface with contacts thereon and a package element having a central region attached to the chip and a peripheral region extending outwardly away from the chip in horizontal directions generally parallel to the front face of the chip;

(b) a substantially imperforate dielectric element overlying the subassembly, the sheet including a central region overlying the central region of the package element adjacent the chip, and a peripheral region extending outwardly from the central region of the sheet and overlying the peripheral region of the package element, the sheet having a top surface facing away from the subassembly and a bottom surface facing toward the subassembly and electrically conductive terminals on the top surface, at least some of the terminals being disposed in said peripheral region of the sheet;

(c) a compliant layer disposed between the subassembly and dielectric element and supporting the dielectric element above the subassembly; and

(d) vertically-extensive flexible first leads embedded in said compliant layer and extending upwardly from the contacts on the chip to the central region of the dielectric element, the flexible leads being electrically connected to the terminals.

3. (new) A packaged semiconductor chip comprising:

(a) a first semiconductor chip having a front face, a rear face, edges bounding said faces and contacts exposed at said front surface;

(b) a chip carrier having inner and outer surfaces, the inner surface of said chip carrier facing in an upward direction toward said chip, the outer surface of said chip carrier facing in a downward direction away from said chip, said chip carrier having a plurality of terminals exposed at said outer surface, at least some of said terminals being electrically connected to at least some of said contacts of said chip; and

(c) a heat sink disposed beneath said chip in thermal communication with a face of said chip, said heat sink being exposed at said outer surface of said chip carrier.

4. (new) A packaged semiconductor chip as claimed in claim 3 wherein said chip carrier includes a peripheral region projecting outwardly beyond the edges of the chip and at least some of said terminals are disposed in said peripheral region.

5. (new) A packaged semiconductor chip as claimed in claim 3 wherein said chip carrier has a hole extending through it from said inner surface to said outer surface and said heat sink is exposed to said outer surface through said hole.

6. (new) A packaged semiconductor chip as claimed in claim 5 wherein said heat sink projects downwardly through said hole.

7. (new) A packaged semiconductor chip as claimed in claim 3 wherein said front face of said chip faces downwardly toward said chip carrier.

8. (new) A packaged semiconductor chip as claimed in claim 3 further comprising a metallic element extending above said first semiconductor chip.

9. (new) A packaged semiconductor chip as claimed in claim 8 wherein said metallic element has side walls projecting downwardly toward said chip carrier.